AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0008] as follows:

[0008] A high-voltage signal HVIN activates transmitter circuit 145 when brought high to pass the verify signal VFY to steering logic 140. As explained below in connection with Figure 1B, high-voltage signal HVIN is even higher than the maximum verify voltage VFY, and consequently approaches a level that might damage circuits -- such as delicate gate oxides -- internal to input circuit 125. High-voltage signal HVIN is therefore brought onto CPLD 100 via a dedicated pin ~~120~~ 121.

Please amend paragraph [0011] as follows:

[0011] Unfortunately, input circuits 125 in state-of-the-art CPLDs may contain device features too small to accommodate the relatively high voltage HVIN required on device pin ~~120~~ 121. For example, if I/O circuits 105 are manufactured using a conventional 0.18-micron process, voltages over about 5 volts can damage input transistors within input circuit 125. The maximum verify voltages VFY required for memory cells 110 in such circuits is approximately 4.5 volts, so verify voltages VFY can be connected to the input terminal of input circuit 125 as shown; however, the threshold voltage required to pass a 4.5 volt signal through transistor 145 without substantial degradation will be approximately 6 or 7 volts. A dedicated device pin ~~120~~ 121 is therefore provided to convey this relatively high voltage ~~HUIN~~ HVIN.

Please amend paragraph [0012] as follows:

[0012] Integrated circuits are becoming ever more densely populated as processing technology improves. As circuit features grow smaller, the number of physical pads that fit on the die surface becomes a limiting factor on the amount of

logic instantiated on a circuit die. Due to the pad-limited nature of modern devices, device pins are at a premium. It is therefore undesirable to provide a dedicated pin ~~120~~ 121 for the purposes of test at the expense of a general purpose I/O circuit 105.